DETECTION PROBABILITY OF INTERCONNECT OPENS USING STUCK-AT TESTS

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Shalini Ghosh

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The thesis of Shalini Ghosh is approved:

F. Joel Ferguson, Chair

Tracy Larrabee

Sreejit Chakravarty

Dean of Graduate Studies
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Abstract

Detection probability of interconnect opens using stuck-at tests

by

Shalini Ghosh

An interconnect break is a break that occurs in the interconnect wiring, which results in logic gate inputs being disconnected from the drivers and causes the wire to float. Interconnect breaks are the most common types of breaks in modern CMOS integrated circuits, so testing and detecting these breaks has become very important.

This thesis models the conditions required for stuck-at tests to detect interconnect breaks in a circuit. We do a worst-case analysis of the detection of these breaks and calculate the minimum length of a test vector required to detect such defects with a specified confidence level, using n-detection principles.

To enhance the understanding of the faulty behavior of the circuit, this thesis presents a statistical model with certain simplifying assumptions based on the length distribution of the wires surrounding the floating wire. From the model, we compute the detection probabilities of such breaks and show that the worst case of detection is when the bias voltage is the logic threshold voltage.
This thesis is dedicated to my beloved Mom, Dad, Rajib and Sugato.
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Chapter 1

Introduction

According to Hawkins, et al. [1], the three classes of defects that can occur during the manufacturing process of an integrated circuit (IC) are:

1. Bridge defects

2. Open circuit (break) defects

3. Parametric delay defects

This thesis is concerned with the second category, open circuits. Open circuits are caused by breaks in the conducting material of a circuit layout due to spot defects, which are primarily lithography related [15], or due to other masking or fabrication errors. Based on their location in a layout, breaks can be categorized into four types [5]:

1. A break that occurs in the interconnect wiring, resulting in logic gate inputs being disconnected from their drivers, and thus causing the wire to float, is called an interconnect break.
2. A break that occurs inside a CMOS cell, affecting the connection between the transistor drain and source, is called a network break.

3. A break that occurs inside a CMOS cell that can affect the connection between the bulk of a n-channel transistor and Gnd, or the bulk of a p-channel transistor and V_{dd}.

4. A break which can disconnect a single transistor gate and its driver [9, 14].

In modern IC’s, as the number of layers of metal have increased, so has the interconnect wiring, which results in a higher probability for interconnect breaks. According to Thompson, the number of vias far exceed the number of transistors and these vias are particularly susceptible to opens [4]. This makes testing and detection of interconnect breaks all the more important. This thesis addresses interconnect breaks.

Konuk, in his Ph.D dissertation [5], described a fault simulation algorithm for detecting interconnect opens, which takes into account the following factors:

- Capacitance between the floating wire (FW) and surrounding wires,

- Miller (gate/drain, gate/source) capacitances to the FW,

- Charge collector diodes, and

- Trapped charge deposited on the FW during fabrication.

The above factors are used by the algorithm to calculate trapped charge intervals on the FW, for a set of stuck-at tests. The fault simulation algorithm computes the following:

- Maximum trapped charge on the FW with which the given test set can detect the open as a stuck-at-0 fault (Q_{max,sa0}), and
• Minimum trapped charge on the FW with which the given test set can detect the open as a s-a-1 fault \(Q_{\text{min,sa1}}\).

If the fault simulator determines that \(Q_{\text{max,sa0}} > Q_{\text{min,sa1}}\), then the interconnect break would have been detected and the fault dropped. In his dissertation, Konuk deals with the detection intervals for trapped charge, but mentions that it would be ideal to consider the detection probabilities instead. Konuk’s fault simulator required knowing the logic value on each wire adjacent to the FW. This thesis presents a method that uses the probability of detecting interconnect breaks while applying randomly selected \(n\) stuck-at-zero and \(n\) stuck-at-one tests for each fault location in the circuit and uses a statistical model instead.

As mentioned earlier, interconnect opens cause floating gates. According to Xue, et al. [3], such opens can be categorized as:

1. Opens causing floating gates affecting only the subcircuit consisting of p-transistors (p-subcircuit). Figure 1.1 shows an example circuit with this type of open annotated with 1.

2. Opens causing floating gates affecting only the subcircuit consisting of n-transistors (n-subcircuit). Figure 1.1 shows an example circuit with this type of open annotated with 2.

3. Opens causing floating gates affecting both the p-subcircuit and the n-subcircuit. Figure 1.1 shows an example circuit with this type of open annotated with 3.

Maly [16] observed that an interconnect open affecting either the p-subcircuit or the n-subcircuit does not hinder the functional behavior of the circuit, except for some
Figure 1.1: A symbolic CMOS circuit showing the location of the three possible classes of interconnect opens.

Changes in the circuit delay. However, an open affecting both the p-subcircuit and the n-subcircuit affects the whole charging and discharging path between the ground and $V_{dd}$ planes and thus causes the circuit to function incorrectly. Therefore, in this model we consider the latter type of interconnect open, which causes floating gates that affect both the p-subcircuit and the n-subcircuit.

The organization of the remaining chapters is as follows:

- Chapter 2 models the conditions required for stuck-at tests to detect interconnect breaks in a circuit.

- Chapter 3 does a worst-case analysis of the detection of these breaks and calculates the minimum length of a test vector required to detect such defects with a specified confidence level, using n-detection principles.
• Chapter 4 presents a statistical model with certain simplifying assumptions, based on the length distribution of the wires surrounding the floating wire. We compute the detection probabilities of such breaks using this model and show that the worst case of detection is when the bias voltage is the logic threshold voltage.

• Chapter 5 summarizes the conclusions that can be drawn from this thesis and provides suggestions for future work.
Chapter 2

Modeling the conditions for detecting a break using stuck-at tests

In Figure 2.1, the trapped charge on the FW ($Q_{\text{trapped}}$) equals the charge on the wiring ($Q_{\text{wire}}$) plus the charge on the gates of the transistors that the FW is connected to ($Q_{\text{gate}}$). That is,

$$Q_{\text{trapped}} = Q_{\text{wire}} + Q_{\text{gate}},$$

where $Q_{\text{gate}}$ determines the logic value of the output of the gate. Since trapped charge is a constant, if more charge resides in the wiring, then less charge is present on the gate, resulting in a certain logic value at the output. If the charge was distributed in the opposite way, then the logic value on the output would be opposite. Thus given a $Q_{\text{trapped}}$, the logic value of the output of a gate with a floating input depends on $Q_{\text{wire}}$. $Q_{\text{wire}}$ depends on
the capacitance and voltage on the surrounding wires, which are either at $V_{dd}$ or $Gnd$ in digital circuits. In Figure 2.2, $C_{in,V_{dd}}$ and $C_{in,Gnd}$ are the total capacitances of the FW to the surrounding signal wires at logic one and logic zero respectively, while $C_{gs,p}$ and $C_{gd,p}$ are the capacitances of the gate to the source and gate to the drain of the p-transistor, respectively. $C_{gs,n}$ and $C_{gd,n}$ are analogous for the n-transistor.

In this analysis, we make the following simplifying assumptions:

1. The interconnect open is assumed to be open-circuit with infinite resistance.

2. In considering the effect of the surrounding wires, we actually consider the capacitive coupling effect due to only the wires adjacent to the FW. This is a reasonable assumption, considering the fact that wires not adjacent to the floating wire would not have a significant effect compared to the effect due to the adjacent wires, as capacitance falls off quickly with distance and increased shielding.

3. $C_{gs,p}$ and $C_{gd,p}$ are negligible compared to $C_{in,V_{dd}}$ and $C_{in,Gnd}$. This is because as
Figure 2.2: Important capacitances in an Inverter with FW.

the sizes of transistor gates are decreasing and interconnect wiring capacitance is increasing, gate capacitances are becoming negligible compared to surrounding wire capacitances.

4. All adjacent wires are equidistant from the FW, as is usually the case with most routers.

5. The threshold voltage $V_{TH}$ is same for all gates, and is approximately equal to $\frac{V_{DD}}{2}$.

6. The capacitance per unit length of the surrounding wires is constant, based on the assumption that all wires adjacent to the floating wire are equidistant from it. We can say that capacitance is directly proportional to the length. Here, by length of a surrounding wire, we mean the length of it that is adjacent to the FW.

From the above assumptions, if a test results in more surrounding wire lengths
at logic zero than at logic one, then $C_{in,Gnd}$ will be greater than $C_{in,V_{dd}}$. This will attract positive charge to the wire ($Q_{wire}$ increases), which pulls charge away from the gates ($Q_{gate}$ decreases) and as a result the p-transistor may be turned on, while the n-transistor may be turned off. This would make the output logic value of the affected gate a logic one. If the test also results in a sensitized path from the gate’s output to a primary output, this is a test for the $FW_{sa0}$. By similar logic, if there were more surrounding wires at logic one and a sensitized path from the gate to a primary output, then it is a test for the $FW_{sa1}$.

This is true for any fully-complementary CMOS gate when the other inputs of the circuit, other than the $FW$, sensitize the output of the gate to the value on the $FW$. This is a necessary condition for all stuck-at tests. ¹

¹Note that interconnect opens causing floating gates are different from the stuck-open, which is a high-impedance state caused by a faulty pull-up or pull-down transistor network in a CMOS gate [11, 16, 8, 9, 2].
Chapter 3

Detection probabilities

Let

- the probability of detecting the break by applying a randomly selected \text{sa0} test,
  \[ P(\text{detected}|\text{sa0 test}) = \alpha, \]

- the probability of detecting the break by applying a randomly selected \text{sa1} test,
  \[ P(\text{detected}|\text{sa1 test}) = \beta, \]

- the probability of not detecting the break by applying a randomly selected \text{sa0} test,
  \[ P(\text{not detected}|\text{sa0 test}) = 1 - \alpha = \alpha', \text{ and} \]

- the probability of not detecting the break by applying a randomly selected \text{sa1} test,
  \[ P(\text{not detected}|\text{sa1 test}) = 1 - \beta = \beta'. \]

We assume that the logic values of the wires during one test are independent of the values of the wires during another test. Thus, the distribution of logic values on the wires is independent of whether a \text{sa0} or a \text{sa1} test is applied. In this case, \( \alpha + \beta = 1. \)
Then \( P(\text{not detected} | \text{sa1 test}) = \beta' = \alpha \) and \( P(\text{not detected} | \text{sa0 test}) = \alpha' = \beta \). This is true because the same length of adjacent wires needs to be at a logic 0 for the \( FW \) to be at logic 0 so that we can detect the \( FW \) as a \( \text{sa0} \) fault as cause it to not be detected as a \( \text{sa1} \) fault. If a break is not detected by a set of one \( \text{sa0} \) and one \( \text{sa1} \) test, then the test for the \( \text{sa0} \) and the \( \text{sa1} \) test must have both failed (i.e. not detected the break). Let the probability of not detecting the break by applying a randomly selected \( \text{sa1} \) test and one randomly selected \( \text{sa1} \) test be \( P(\text{not detect break} | 1 \text{ sa0} \land 1 \text{ sa1}) \). This fact results in,

\[
P(\text{not detect break} | 1 \text{ sa0} \land 1 \text{ sa1}) = P(\text{not detected} | \text{sa1 test} \land \text{not detected} | \text{sa0 test}).
\]

Since we assume that the values on the wires during one test is independent of the values on the wires during another test,

\[
P(\text{not detect break} | 1 \text{ sa0} \land 1 \text{ sa1}) = P(\text{not detected} | \text{sa1 test}) \times P(\text{not detected} | \text{sa0 test}).
\]

Putting in the values for these two probabilities we get,

\[
P(\text{not detect break} | 1 \text{ sa0} \land 1 \text{ sa1}) = \beta' \cdot \alpha'.
\]

When \( \alpha + \beta = 1 \),

\[
P(\text{not detect break} | 1 \text{ sa0} \land 1 \text{ sa1}) = \beta' \cdot \alpha' = \alpha \cdot \beta = \alpha (1 - \alpha) = \alpha - \alpha^2.
\]

To find when this value is a maximum, we take the derivative and set it to zero. That is,

\[
\frac{d(\alpha - \alpha^2)}{d\alpha} = 1 - 2\alpha = 0.
\]

This results in \( \alpha = \frac{1}{2} \); that is, \( P(\text{not detect break} | 1 \text{ sa0} \land 1 \text{ sa1}) \) is maximum when the \( P(\text{detected} | \text{sa0 test}) = \frac{1}{2} \). This can be seen in Figure 3.1, which shows \( P(\text{not detect break} | 1 \text{ sa0} \land 1 \text{ sa1}) \) as a function of \( \alpha \).
Figure 3.1: Probability of not detecting the break fault versus varying $\alpha$, when one sa0 test and one sa1 test are applied.

Now, if we apply $n$ sa0 tests and $n$ sa1 tests ($n$-detection) [7, 10], then the probability of not detecting the break falls off as $(\alpha \beta)^n$. We can explain this as follows: Each of the $n$ sa1 tests has a $P$(not detected|sa1 test) $= \alpha$ and each of the $n$ sa0 tests has a $P$(not detected|sa0 test) $= \beta$. Assuming all tests are independent, the total $P$(not detect break|n sa0 $\land$ n sa1) $= (\alpha \beta)^n$. Figure 3.2 illustrates this effect. Thus, with $n$ sa0 and $n$ sa1 tests, the probability of detecting the break approaches one as $n$ increases.

If instead, we apply $n$ sa1 tests and $m$ sa0 tests, then using differential calculus we can say that $P$(not detect break|n sa0 $\land$ m sa1) $= (\alpha^n \beta^m)$ is maximum for $\alpha = \left(\frac{n}{n+m}\right)$.

Under certain conditions, the assumption that $\alpha + \beta = 1$ and consequently $\alpha' + \beta' = 1$ might not be true. Due to dependencies between logic values in different wires, $\alpha' + \beta'$ might deviate slightly from 1. We illustrate one situation in which this kind of dependency may arise. Consider Figure 3.3, where we have the floating wire $FW$ connected
Figure 3.2: Probability of not detecting the break versus varying $n$, when $n$ sa0 and $n$ sa1 tests are applied.

to the output of an OR-gate. Without dependencies between wires, that is, without capacitive coupling between adjacent wires, by previous assumption, we have $\beta' = 1 - \alpha'$. Let $\alpha' = x$. Therefore, $\beta' = (1 - x)$. Now to test the FW with a sa0 test, we will have to put a 1 on one of the input wires, that is, on either $a$ or $b$. The possible input combinations are 10,01,11. Thus we see that $\frac{2}{3}$ of the time, the input wire $b$ will have a 1 on it. If wire $b$ is adjacent to the FW, then there will be capacitive coupling as shown in Figure 3.4. When $b$ has a 1 on it, then the voltage on the FW will increase $\frac{2}{3}$ of the time. Thus in this case the sa0 test is more likely to fail in detecting the break due to tendency of wire $b$ having a one on it and increasing the voltage on the FW. This implies that $P(FW = 1 | sa0$ test) \(\equiv P(\text{not detected} | sa0 \text{ test}) = \alpha' \) increases by an amount say $\delta$, where $0 < \delta < 1$. Therefore, $\alpha' = x + \delta$. Again, to test the FW with a sa1 test, we will have to put a 0 on both the input wires, that is, on $a$ and $b$. Now, when $b$ has a 0 on it, then due to capacitive
coupling between adjacent wires, the $FW$ will tend to have a 0 on it [Figure 3.4]. Thus in this case the sa1 test is more likely to fail in detecting the break, which implies that $P(\text{not detected}|\text{sa1 test})(\beta')$ increases by an amount, say $\epsilon$, where $0 < \epsilon < 1$. Therefore, 

$$\beta' = (1 - x) + \epsilon.$$ 

Hence in this case $\alpha' + \beta' = 1 + \delta + \epsilon = k_2$, where $k_2 > 1$. With similar logic we can argue that there are cases in which $\alpha' + \beta' = k_1$, where $k_1 < 1$.

Thus, taking dependency into account we can have $\alpha' + \beta' \neq 1$. To solve the problem of finding the worst-case detection probability when $\alpha' + \beta' \neq 1$, we find the maximum value of $P(\text{not detect break}|1 \text{ sa0} \land 1 \text{ sa1}) = \alpha'\beta' = z$ (say), subject to the constraint equation $k_1 < (\alpha' + \beta') < k_2$, where $k_1 < 1 < k_2$.

Figure 3.5 shows the 3-D plot of the curve $z = \alpha'\beta'$, plotted in MATLAB. We observe that the contours of $z$ are a set of hyperbolas on the $(\alpha', \beta')$ plane, having the form $\alpha'\beta' = \text{constant} = c$, as shown in Figure 3.6. Since $\alpha', \beta'$ are probability values, $\alpha', \beta'$ lie between 0 and 1. So we consider the nature of the curves in the first quadrant only. Figure 3.7 shows the curves for two given hyperbolas $\alpha'\beta' = c_1$ and $\alpha'\beta' = c_2$, where
$c_2 > c_1$.

So, the maximum z-value in the constraint region $b-c-d-e-g-h$, as shown in Figure 3.8, would lie along the contour hyperbola that is tangential to the line $\alpha' + \beta' = k_2$, shown in Figure 3.8 as the line $a-h-g-f$. We obtain the point of intersection of the hyperbola with the line by solving the equation $\alpha'\beta' = c$ and $\alpha' + \beta' = k_2$. This gives:

$$\alpha' = \frac{k_2 \pm \sqrt{k_2^2 - 4c}}{2},$$

$$\alpha' = \beta' = \frac{k_2}{2} \text{ if } c = \frac{k_2^2}{4c}$$

Therefore, the maximum-z point in the constraint region is the point of intersection of the hyperbola $\alpha'\beta' = k_2^2/4$ with the line $\alpha' + \beta' = k_2$, which is tangential to it. The co-ordinates of the point of intersection are $(k_2/2, k_2/2)$.

Now if $d_n^f$ be the $n$-step detection probability [6] that we detect a break $f$ (at least once) by applying $n$ sa0 and $n$ sa1 tests with $P(\text{not detected|sa0 test}) = \alpha'$ and
Figure 3.5: Surface and contour plot for $z = \alpha' \beta'$. The X and the Y axes represent $\alpha'$ and $\beta'$ respectively, while the Z axis represents $z$.

\[ P(\text{not detected}|\text{sa1 test}) = \beta', \text{ then} \]

\[ d_n^l = 1 - (\alpha' \beta')^n. \]

The detection quality $d_n$ of a test sequence is the lowest $n$-step detection probability among the stuck-at faults in the circuit. Therefore,

\[ d_n = \min_f d_n^l = 1 - [(\alpha' \beta')_{max}]^n. \]

Thus the above formula determines the detection quality of the tests.

To determine the number of sa0 and sa1 tests, $n$, required to achieve a level of confidence of at least $c$ in detecting a break, choose $n$ to satisfy

\[ d_n \geq c. \]
Figure 3.6: Contours of equal $z$ values for $z = \alpha' \beta'$. 
**Figure 3.7**: Curves of $\alpha' \cdot \beta' = c$, where $0 < \alpha', \beta' < 1$.

**Figure 3.8**: Curves of $k_1 \leq \alpha' + \beta' \leq k_2$, where $0 < \alpha', \beta' < 1$. 
This is justified because the test length that is long enough to detect the most difficult break with probability \(c\) will detect any other break \(f\) with \(d_f^f \geq c\) [6]. Therefore,

\[
1 - ((\alpha' \beta')_{\text{max}})^n \geq c,
\]

\[
((\alpha' \beta')_{\text{max}})^n \leq 1 - c. \tag{3.1}
\]

Taking the natural logarithm of both sides of Equation 3.1:

\[
\ln((\alpha' \beta')_{\text{max}})^n \geq \ln(1 - c),
\]

\[
n \geq \frac{\ln(1 - c)}{\ln((\alpha' \beta')_{\text{max}})}. \tag{3.2}
\]

Thus from Equation 3.2, the lowest value of \(n\) required to achieve a confidence level of at least \(c\) in detecting a break is:

\[
n_t = \left\lceil \frac{\ln(1 - c)}{\ln((\alpha' \beta')_{\text{max}})} \right\rceil. \tag{3.3}
\]

Now, if there are \(F\) breaks in the circuit under test, with probability of not being detected by a sa0 and a sa1 test equal to \((\alpha' \beta')_{\text{max}}), then to detect all the \(F\) breaks with a confidence level of at least \(c\),

\[
\{1 - ((\alpha' \beta')_{\text{max}})^n\}^F \geq c,
\]

\[
1 - ((\alpha' \beta')_{\text{max}})^n \geq c^{\frac{1}{F}},
\]

\[
((\alpha' \beta')_{\text{max}})^n \leq 1 - c^{\frac{1}{F}},
\]

\[
n \geq \frac{\ln(1 - c^{\frac{1}{F}})}{\ln((\alpha' \beta')_{\text{max}})}. \tag{3.4}
\]

Thus from Equation 3.4, the lowest value of \(n\) required to achieve a confidence level of at least \(c\) in detecting all the \(F\) breaks is:

\[
n_{\text{min}} = \left\lceil \frac{\ln(1 - c^{\frac{1}{F}})}{\ln((\alpha' \beta')_{\text{max}})} \right\rceil. \tag{3.5}
\]
EXAMPLE 1: If \((a^\prime b^\prime)_{max} = 0.5 \times 0.5 = 0.25\) and \(c = 0.99\), then, from Equation 3.3, \(n_l = 4\). Thus in this case, when the worst case probability of the break being not detected with a sa0 and a sa1 test is 0.25, we need minimum 4 sa0 and 4 sa1 tests to detect the break with a confidence level of 0.99.

EXAMPLE 2: If there are 100 nodes in the circuit that may have breaks, that is, if \(F = 100\) and if the probability of not detecting each of the breaks, that is, \((a^\prime b^\prime)_{max} = 0.5 \times 0.5 = 0.25\) and \(c = 0.99\), then, from Equation 3.5, \(n_{min} = 7\). Thus in this case, when the worst case probability of the most difficult to detect break being not detected with a sa0 and a sa1 test is 0.25, we need minimum 7 sa0 and 7 sa1 tests to detect all the breaks in the circuit with a confidence level of 0.99.

The above examples show that the understanding of the detection of interconnect opens must be refined from the current worst-case analysis to obtain more useful lower bounds on the number of stuck-at tests needed for their detection. Note that even if \((a^\prime b^\prime)_{max} = 0.4 \times 0.6 = 0.24\), there is very little change in \(n_{min}\).
Chapter 4

Estimating detection probabilities

To enhance the understanding of the faulty behavior of the circuit, we use the fact that capacitance is proportional to length and construct a length distribution model, using independence of values on the wires. To get an estimate of $\alpha$ and $\beta$ from our model, we would like to estimate:

- the probability that $\left(\frac{C_{in, V_{dd}}}{C_{in, V_{cc}} < 1}\right)$, to calculate $\alpha$, and

- the probability that $\left(\frac{C_{in, V_{dd}}}{C_{in, V_{cc}} > 1}\right)$, to calculate $\beta$.

From the assumptions made in this thesis, capacitance is directly proportional to the wire length. Thus we can estimate the probability of detecting an interconnect break with stuck-at tests by using the probability distribution of the ratio of total length of surrounding wires at logic one ($T_{Hi}$) to the total length of all surrounding wires ($T_i$).

The voltage on the floating wire without capacitance from the signal wires is important in determining $\alpha$ and $\beta$. We call this the bias voltage. How far the bias voltage is from the threshold voltage is a function of the trapped charge on the floating wire, the
transistor capacitances and the FW's capacitance to the ground and \( V_{dd} \) planes.

We assume the worst case, that the bias voltage is the logic threshold voltage, which means the trapped charge is small [5]. This being the worst case can be easily understood by noting that the presence of trapped charge would either increase \( P(\text{detected}|s_a0 \text{ test}) \) or \( P(\text{detected}|s_a1 \text{ test}) \), in either case causing \( P(\text{not detect break } | s_a0 \wedge 1 \text{ sa0}) \) to move away from the worst case of detection, that is, from \( \alpha = \beta = 0.5 \).

4.1 Analysis of the model

Consider the following. Let there be \( n \) signal wires that can affect the charge on the FW. Let each of the \( n \) wires have individual lengths. Out of these \( n \) wires, let \( k \) wires be at logic one. The probability distribution of \( k \) is binomial. This is because we assume that the logic value of any of the wires is independent of the other wires' logic values and we can randomly choose a wire from the set of \( n \) wires and add it to the set of \( k \) wires if it is at logic one. So this is a series of Bernoulli trials, which gives a binomial distribution.

In order to find the probability \( P(T_{l1}) \), of \( k \) wires at logic 1 adding up to a total length \( T_{l1} \), we see that the total probability of wires at logic one adding up to \( T_{l1} \) is

\[
P(T_{l1}) = P(k = 0) \cdot P(0 \text{ wires add to } T_{l1}) \\
+ P(k = 1) \cdot P(1 \text{ wire is } T_{l1}) \\
+ P(k = 2) \cdot P(2 \text{ wires add to } T_{l1}) \\
+ \ldots \\
+ P(k = n) \cdot P(n \text{ wires add to } T_{l1})
\]
\[
= \sum_{k=0}^{n} \left[ B_k(n, p) \cdot P\left( \sum_{i=1}^{k} l_i = T_{i1} \right) \right],
\]

(4.1)

where

- \( l_i \) is the length of the \( i^{th} \) wire, and

- \( B_k(n, p) \) is the probability mass function of a \( k \)th binomial random variable with parameters \((n, p)\), such that

\[
B_k(n, p) = \frac{n!}{k!(n-k)!} p^k (1-p)^{n-k}.
\]

(4.2)

In this equation, \( p \) equals the probability that a wire chosen at random from \( n \) wires is at logic 1.

From the theory of discrete convolutions [13, 12],

\[
\left( \sum_{i=1}^{k} l_i = T_{i1} \right) = \sum_{a_1=l_{min}}^{l_{max}} \sum_{a_2=l_{min}}^{l_{max}} \ldots \sum_{a_{k-1}=l_{min}}^{l_{max}} P(l_1 = a_1) \ldots P(l_{k-1} = a_{k-1}) \cdot P(l_k = T_{i1} - a_1 - \ldots - a_{k-1}).
\]

(4.3)

We can also find the distribution of total lengths of wires at logic zero \((T_{i0})\),

\[
P(T_{i0}) = \sum_{k=0}^{n} \left[ B_{n-k}(n, 1-p) \cdot P\left( \sum_{i=1}^{n-k} l_i = T_{i0} \right) \right].
\]

(4.4)

To get an idea of the distribution of the total lengths of all surrounding wires \((T_i)\) we use the fact that \( l_1 + l_2 + \ldots + l_n = T_i \). Again using the theory of discrete convolutions [13, 12] we get:

\[
P(l_1 + \ldots + l_n = T_i) = \sum_{a_1=l_{min}}^{l_{max}} \sum_{a_2=l_{min}}^{l_{max}} \ldots \sum_{a_{n-1}=l_{min}}^{l_{max}} P(l_1 = a_1) \ldots P(l_{n-1} = a_{n-1}) \cdot P(l_n = T_i - a_1 - \ldots - a_{n-1}).
\]
This gives an idea about the total lengths possible but does not say anything about the actual total lengths permitted given specific values for \( T_{l1} \). Because of this we need to derive the probability of the ratio \( \frac{T_{l1}}{T_l} \), where \( T_{l1} \leq T_l \).

### 4.1.1 Derivation of Probability of \( \frac{T_{l1}}{T_l} \)

To arrive at the probability distribution for \( \frac{T_{l1}}{T_l} \), where \( T_{l1} \leq T_l \), we calculate the probability for \( \frac{T_{l1}}{T_l} = \lambda \) as follows:

There are two cases for \( \lambda \):

- When \( \lambda \neq 0 \), we have to calculate the probability for each value of \( T_{l1} = m \) (\( 1 \leq m \leq n_{l_{\text{max}}} \)) and the corresponding value for \( T_l = \frac{1}{\lambda}m = \gamma m \), given \( T_l \geq T_{l1} \), that is, \( \gamma \geq 1 \), where \( \gamma = 1/\lambda \).

- When \( \lambda = 0 \), we have to calculate the probability when \( T_{l1} = 0 \), for all values of \( T_l \), given \( \gamma > 1 \) (all wires are at logic one).

Therefore,

\[
P \left( \frac{T_{l1}}{T_l} = \lambda \right) = \begin{cases} 
\sum_{u=n_{l_{\text{min}}}}^{n_{l_{\text{max}}}} P \left( T_{l1} = 0, T_l = u | \gamma > 1 \right), \lambda = 0 \\
\sum_{m=l_{\text{min}}}^{n_{l_{\text{max}}}} P \left( T_{l1} = m, T_l = \frac{1}{\lambda}m | \gamma \geq 1 \right), \lambda \neq 0 
\end{cases}
\]

**Case 1 (\( \lambda = 0 \)):

\[
P \left( \frac{T_{l1}}{T_l} = \lambda \right) = \sum_{u=n_{l_{\text{min}}}}^{n_{l_{\text{max}}}} \frac{P \left( T_{l1} = 0, T_l = u, \gamma > 1 \right)}{\gamma > 1}.
\]  \hspace{2cm} (4.5)

Using the following chain rule of conditional probability to expand the numerator
of equation 4.5,

\[
P(A, B, C) = P(A) \cdot P(B, C | A)
\]

\[
= P(A) \cdot P(B | A) \cdot P(C | B, A).
\]  \hspace{1cm} (4.6)

This results in,

\[
P \left( \frac{T_{II}}{T_I} = \lambda \right) = \sum_{u = n_{l_{min}}}^{n_{l_{max}}} \frac{P(T_{II} = 0) \cdot P(T_i = u | T_{II} = 0) \cdot P(\gamma > 1 | T_{II} = 0, T_I = u)}{P(T_I > T_{II})} \\
= \frac{P(T_{II} = 0)}{P(T_I > T_{II})} \left[ \sum_{u = n_{l_{min}}}^{n_{l_{max}}} P(T_i = u | T_{II} = 0) \right] \\
= \frac{P(T_{II} = 0)}{P(T_I > T_{II})},
\]

since \[
\sum_{u = n_{l_{min}}}^{n_{l_{max}}} P(T_i = u | T_{II} = 0) = 1.
\] \hspace{1cm} (4.7)

**Case 2** \((\lambda \neq 0)\):

Using the conditional probability rule again to obtain a more workable equation,

\[
P \left( \frac{T_{II}}{T_I} = \lambda \right) = \sum_{m = l_{min}}^{l_{max}} \frac{P(T_i = \gamma m, T_{II} = m, T_I \geq T_{II})}{P(T_I \geq T_{II})} \quad \text{for } \lambda \neq 0.
\] \hspace{1cm} (4.8)

Using the chain rule of conditional probability from Equation 4.6 to expand the numerator of Equation 4.8,

\[
P(T_i = \gamma m, T_{II} = m, T_I \geq T_{II}) = P(T_I = \gamma m) \cdot P(T_{II} = m | T_I = \gamma m) \cdot P(T_I \geq T_{II} | T_I = \gamma m, T_{II} = m)
\]

\[
= P(T_I = \gamma m) \cdot P(T_{II} = m | T_I = \gamma m) \cdot P(\gamma \geq 1 | T_I = \gamma m, T_{II} = m)
\]

\[
= P(T_I = \gamma m) \cdot P(T_{II} = m | T_{II} + T_{b0} = \gamma m).
\]
\begin{equation}
P(\gamma \geq 1 | T_i = \gamma m, T_{l1} = m)
\end{equation}

[since \( T_i = T_{l1} + T_{l0} \)]

\begin{equation}
= P(T_i = \gamma m) \cdot P(T_{l1} = m | T_{l1} + T_{l0} = m + (\gamma - 1)m) \cdot P(\gamma \geq 1 | T_i = \gamma m, T_{l1} = m)
\end{equation}

[since \( \gamma m = m + (\gamma - 1)m \)].

Now, for two random variables \( X \) and \( Y \), by Bayes’ Theorem, we have,

\begin{equation}
P(X = x | X + Y = x + y) = \frac{P(X + Y = x + y | X = x)P(X = x)}{P(X + Y = x + y)}
\end{equation}

\begin{equation}
= \frac{P(Y = y | X = x)P(X = x)}{P(X + Y = x + y)}
\end{equation}

\begin{equation}
= \frac{P(Y = y, X = x)}{P(X + Y = x + y)}
\end{equation}

[since \( P(A, B) = P(A | B)P(B) \)]

\begin{equation}
= \frac{P(X = x, Y = y)}{P(X + Y = x + y)}
\end{equation}

[since \( P(BA) = P(AB) \)].

Using, Equation 4.10, from Equation 4.9,

\begin{equation}
P(T_i = \gamma m, T_{l1} = m, T_i \geq T_{l1}) = P(T_i = \gamma m) \cdot \frac{P(T_{l1} = m, T_{l0} = (\gamma - 1)m)}{P(T_i = \gamma m)} \cdot P(\gamma \geq 1 | T_i = \gamma m, T_{l1} = m)
\end{equation}

\begin{equation}
= P(T_{l1} = m, T_{l0} = (\gamma - 1)m) \cdot P(\gamma \geq 1 | T_i = \gamma m, T_{l1} = m).
\end{equation}

Thus, from Equation 4.8 and Equation 4.11,

\begin{equation}
P \left( \frac{T_{l1}}{T_i} = \lambda \right) = \sum_{m=\ell_{\text{min}}}^{\ell_{\text{max}}} \left[ \frac{P(T_{l1} = m, T_{l0} = (\gamma - 1)m)P(\gamma \geq 1 | T_i = \gamma m, T_{l1} = m)}{P(T_i \geq T_{l1})} \right].
\end{equation}
Now, to find \( P(T_{i_1} = m, T_{i_0} = (\gamma - 1)m) \), we see that this is the joint probability distribution for \( T_{i_1} \) and \( T_{i_0} \). We look at the problem this way: Out of \( n \) wires, for \( k \) wires to be at logic one, the probability is \( B_k(n, p) \) (as explained in Section 4.1). Now the lengths of the \( k \) wires have to add up to \( m \), while the lengths of the \((n - k)\) wires have to add up to \((\gamma - 1)m\). Without loss of generality, let \( k \) wires out of \( n \) be at logic 1 and we index them from 1 to \( k \). Also we index the \((n - k)\) wires that are at logic 0 from \((k + 1)\) to \( n \). Thus we have,

\[
P(T_{i_1} = m, T_{i_0} = (\gamma - 1)m) = \sum_{k=1}^{n} [P(l_1 + \ldots + l_k = m, l_{k+1} + \ldots + l_n = (\gamma - 1)m) 
\cdot B_k(n, p)]
\]

\[
= \sum_{k=1}^{n} [P(l_1 + \ldots + l_k = m) \cdot P(l_{k+1} + \ldots + l_n = (\gamma - 1)m) 
\cdot B_k(n, p)].
\]  

(4.13)

Thus, from Equations 4.8 and 4.13 we get,

\[
P\left( \frac{T_{i_1}}{T_1} = \lambda \right) = \sum_{m=1}^{n} \sum_{k=1}^{n} [P(l_1 + \ldots + l_k = m) \cdot P(l_{k+1} + \ldots + l_n = (\gamma - 1)m) 
\cdot B_k(n, p)] \cdot \frac{P(\gamma \geq 1 | T_{i_1} = \gamma m, T_{i_0} = m)}{P(T_{i_1} \geq T_{i_0})}.
\]  

(4.14)

Now from the theory of discrete convolution, we get

\[
P(l_1 + \ldots + l_k = m) = \sum_{h_1=1}^{l_{\text{max}}} \sum_{h_2=1}^{l_{\text{max}}} \ldots \sum_{h_{k-1}=1}^{l_{\text{max}}} P(l_1 = h_1) \ldots P(l_k = m - h_1 \ldots h_{k-1}),
\]  

(4.15)

and

\[
P(l_{k+1} + \ldots + l_n = (\gamma - 1)m) = \sum_{g_1=1}^{l_{\text{max}}} \sum_{g_2=1}^{l_{\text{max}}} \ldots \sum_{g_{n-k-1}=1}^{l_{\text{max}}} P(l_1 = g_1) 
\ldots P(l_n = (\gamma - 1)m - g_1 \ldots g_{n-k-1}).
\]  

(4.16)
Using Equations 4.2, 4.15 and 4.16 we can compute the value of \( P \left( \frac{T_{l1}}{T_l} = \lambda \right) \) from Equation 4.14.

In this derivation we have considered the length distribution to be discrete and hence performed discrete convolutions. If the length distribution is continuous, then we do continuous convolutions.

### 4.1.2 Example to demonstrate how the equations work

Consider the following example: let there be three wires \((n = 3)\) with two possible lengths of one or two. Any wire picked at random can be either at logic 1 or at logic 0. We assume that in this case \( p = 0.5 \). Intuitively we know that the probability for the case when \( \left( \frac{T_{l1}}{T_l} = \frac{1}{6} \right) \) is zero. Now we show the computation using the Equation 4.12 in Section 4.1.1:

\[
P \left( \frac{T_{l1}}{T_l} = \frac{1}{6} \right) = \sum_{m=1}^{6} \left[ \frac{P(T_{l1} = m, T_{l0} = (\gamma - 1)m)P(\gamma \geq 1|T_i = \gamma m, T_{l1} = m)}{P(T_i \geq T_{l1})} \right].
\]

For this equation, \( \gamma = 6 \geq 1 \) always, so \( P(\gamma \geq 1|T_i = \gamma m, T_{l1} = m) = 1 \) always.

Therefore \( \left( \frac{T_{l1}}{T_l} = \frac{1}{6} \right) \) = \[
\frac{P(T_{l1} = 1, T_{l0} = 5)}{P(T_i \geq T_{l1})} + \frac{P(T_{l1} = 2, T_{l0} = 10)}{P(T_i \geq T_{l1})} + \frac{P(T_{l1} = 3, T_{l0} = 15)}{P(T_i \geq T_{l1})} + \frac{P(T_{l1} = 4, T_{l0} = 20)}{P(T_i \geq T_{l1})} + \frac{P(T_{l1} = 5, T_{l0} = 25)}{P(T_i \geq T_{l1})} + \frac{P(T_{l1} = 6, T_{l0} = 30)}{P(T_i \geq T_{l1})}.
\]

Now using Equation 4.13 in Section 4.1.1,

\[
P(T_{l1} = m = 1, T_{l0} = (\gamma - 1)m = 5) = P(l_1 = 1)P(l_2 + l_3 = 5)B_1(3, 0.5) + \]

\[
P(l_1 + l_2 = 1)P(l_3 = 5)B_2(3, 0.5) + \]
\[ P(l_1 + l_2 + l_3 = 1)B_2(3, 0.5), \]

but using Equation 4.16 in Section 4.1.1,

\[
P(l_2 + l_3 = 5) = P(l_2 = 1)P(l_3 = 4) + \\
P(l_2 = 2)P(l_3 = 3) + \\
P(l_2 = 3)P(l_3 = 2) + \\
P(l_2 = 4)P(l_3 = 1) \\
= 0 + 0 + 0 + 0 = 0.
\]

By similar logic \( P(l_1 + l_2 = 1) = 0 \), and \( P(l_1 + l_2 + l_3 = 1) = 0 \). Thus, \( P(T_{11} = m = 1, T_{10} = (\gamma - 1)m = 5) = 0 \). Similarly,

\[
\frac{P(T_{11} = 2, T_{10} = 10)}{P(T_i \geq T_{11})} = 0 \\
\frac{P(T_{11} = 3, T_{10} = 15)}{P(T_i \geq T_{11})} = 0 \\
\frac{P(T_{11} = 4, T_{10} = 20)}{P(T_i \geq T_{11})} = 0 \\
\frac{P(T_{11} = 5, T_{10} = 25)}{P(T_i \geq T_{11})} = 0 \\
\frac{P(T_{11} = 6, T_{10} = 30)}{P(T_i \geq T_{11})} = 0.
\]

Hence, \( P(\frac{T_{11}}{T_i} = \frac{1}{5}) = 0 \) for the case of \( \lambda = 1/6 \), as expected.

### 4.1.3 Another Example

Now we compute the total probability distribution for \( (T_{11}/T_i) \) for the following example. Let there be two wires \( (n = 2) \) with possible lengths of one, two and three, with probability of occurring of \( \frac{1}{3}, \frac{1}{3}, \text{and } \frac{1}{3} \), respectively. As before, we consider \( p = 0.5 \). The
Figure 4.1: Probability distributions of (a) lengths of those surrounding wires, and (b) number of surrounding wires at logic one, for the example in Section 4.1.3.

Figure 4.2: The resulting probability distribution for $T_{l1}$ from Equation 4.1 for the example in Section 4.1.3.

Length distribution would look like Figure 4.1(a). With two wires the distribution of $k$ would look like Figure 4.1(b), due to its binomial nature.

For this case, if we compute the distribution for $T_{l1}$, using Equations 4.1, 4.2 and 4.3 in Section 4.1, we would get the graph in Figure 4.2. Table 4.1 shows the computations for the probability distribution of $T_{l1}$.

The next step is to find the probability distribution for the ratio of $(T_{l1}/T_l)$ in Figure 4.3. Table 4.2 shows a sample calculation of $P(\lambda)$ for $\lambda = 1/2$ and Table 4.3 shows
\begin{tabular}{|c|c|c|c|c|}
\hline
$T_{11}$ & $B_0(n, p)$ & $B_1(n, p)$ & $B_2(n, p)$ & $P(T_{11})$ \\
\hline
0 & 0.25 · (1) & 0.50 · (0) & & 0.25 \\
1 & 0.25 · (0) & 0.50 · (0.33) & 0.25 · (0)(0) & 0.17 \\
2 & 0.25 · (0) & 0.50 · (0.33) & 0.25 · (0.33)(0.33) & 0.19 \\
3 & 0.25 · (0) & 0.50 · (0.33) & 0.25 · [(0.33)(0.33) + (0.33)(0.33)] & 0.22 \\
4 & 0.25 · (0) & 0.50 · (0) & 0.25 · [(0.33)(0.33) + (0.33)(0.33) + (0.33)(0.33)] & 0.08 \\
5 & 0.25 · (0) & 0.50 · (0) & 0.25 · [(0.33)(0.33) + (0.33)(0.33)] & 0.06 \\
6 & 0.25 · (0) & 0.50 · (0) & 0.25 · (0.33)(0.33) & 0.03 \\
\hline
\end{tabular}

\textbf{Table 4.1}: All computations for the distribution of $T_{11}$ for the example in Section 4.1.3.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{probability_distribution.png}
\caption{Probability distribution of $(T_{11}/T_i) = \lambda$ for the example in Section 4.1.3.}
\end{figure}

Another sample calculation of $P(\lambda)$ for $\lambda = \frac{2}{3}$. Table 4.4 shows the probability of $(\frac{T_{11}}{T_i} = \lambda)$ for all permitted values of $\lambda$.

From Figure 4.3, we see that $P(\lambda = 0) = 0.25 = P(\lambda = 1)$ is greater than all other $P(\lambda)$ values, as expected.

When we plot the curve of $P(\lambda)$ vs. $\lambda$, the sum of the probabilities of $(T_{11}/T_i)$, when $\lambda > 1/2$, equals $P(\text{detected|sa1 test})$. The sum of the probabilities of $(T_{11}/T_i)$, when $\lambda < 1/2$, equals $P(\text{detected|sa0 test})$.

From Figure 4.3, we see that $P(\lambda) = \frac{1}{6}$ for $\lambda = \frac{1}{2}$. Now, due to noise in the
\[ m \quad k \quad P(l_1 + \ldots + l_k = m) \quad P(l_{k+1} + \ldots + l_n = (\gamma - 1)m) \quad B_k(n, p) \quad T_l \quad xyz \]

<table>
<thead>
<tr>
<th>$m$</th>
<th>$k$</th>
<th>$P(l_1 + \ldots + l_k = m)$</th>
<th>$P(l_{k+1} + \ldots + l_n = (\gamma - 1)m)$</th>
<th>$B_k(n, p)$</th>
<th>$T_l$</th>
<th>$xyz$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>( P(l_1 = 1) = \frac{1}{3} )</td>
<td>( P(l_2 = 1) = \frac{1}{3} )</td>
<td>0.5</td>
<td>2</td>
<td>( \frac{1}{18} )</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>( P(l_1 + l_2 = 1) = 0 )</td>
<td>( P(\text{no wires} = 1) = 0 )</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>( P(l_1 = 2) = \frac{1}{3} )</td>
<td>( P(l_2 = 2) = \frac{1}{3} )</td>
<td>0.5</td>
<td>4</td>
<td>( \frac{1}{18} )</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>( P(l_1 + l_2 = 2) = \frac{1}{5} )</td>
<td>( P(\text{no wires} = 2) = 0 )</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>( P(l_1 = 3) = \frac{1}{3} )</td>
<td>( P(l_2 = 3) = \frac{1}{3} )</td>
<td>0.5</td>
<td>6</td>
<td>( \frac{1}{18} )</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>( P(l_1 + l_2 = 3) = \frac{2}{5} )</td>
<td>( P(\text{no wires} = 3) = 0 )</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>( P(l_1 = 4) = 0 )</td>
<td>( P(l_2 = 4) = 0 )</td>
<td>0.5</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>( P(l_1 + l_2 = 4) = \frac{3}{5} )</td>
<td>( P(\text{no wires} = 4) = 0 )</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>( P(l_1 = 5) = 0 )</td>
<td>( P(l_2 = 5) = 0 )</td>
<td>0.5</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>( P(l_1 + l_2 = 5) = \frac{2}{5} )</td>
<td>( P(\text{no wires} = 5) = 0 )</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>( P(l_1 = 6) = 0 )</td>
<td>( P(l_2 = 6) = 0 )</td>
<td>0.5</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>( P(l_1 + l_2 = 6) = \frac{1}{5} )</td>
<td>( P(\text{no wires} = 6) = 0 )</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
</tbody>
</table>

For \( \lambda = \frac{1}{2} \), \( P(\lambda) = \sum xyz = 3/18 = 1/6 \)

**Table 4.2**: Computation of \( P(\lambda) \) for the case \( \lambda = \frac{1}{2} \) for the example in Section 4.1.3.

\[
<table>
<thead>
<tr>
<th>m</th>
<th>k</th>
<th>P(l_1 + \ldots + l_k = m)</th>
<th>P(l_{k+1} + \ldots + l_n = (\gamma - 1)m)</th>
<th>B_k(n, p)</th>
<th>T_l</th>
<th>xyz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>( \frac{1}{3} )</td>
<td>0</td>
<td>0.5</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>( \frac{1}{3} )</td>
<td>( \frac{1}{3} )</td>
<td>0.5</td>
<td>3</td>
<td>( \frac{1}{18} )</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>( \frac{2}{5} )</td>
<td>0</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>( \frac{1}{3} )</td>
<td>0</td>
<td>0.5</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>( \frac{2}{5} )</td>
<td>0</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0.5</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>( \frac{3}{5} )</td>
<td>0</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0.5</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>( \frac{2}{5} )</td>
<td>0</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0.5</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>( \frac{1}{5} )</td>
<td>0</td>
<td>0.25</td>
<td>-</td>
<td>0</td>
</tr>
</tbody>
</table>

For \( \lambda = \frac{2}{3} \), \( P(\lambda) = \sum xyz = \frac{1}{18} \)

**Table 4.3**: Computation of \( P(\lambda) \) for the case \( \lambda = \frac{2}{3} \) for the example in Section 4.1.3.
\begin{center}
\begin{tabular}{|c|c|}
\hline
\(\lambda\) & \(P\left(\frac{t}{\tau} = \lambda\right)\) \\
\hline
0 & 1/4 \\
1/4 & 1/18 \\
1/3 & 1/18 \\
2/5 & 1/18 \\
1/2 & 1/6 \\
3/5 & 1/18 \\
2/3 & 1/18 \\
3/4 & 1/18 \\
1 & 1/4 \\
\hline
\end{tabular}
\end{center}

\textbf{Table 4.4}: Table showing the permitted values for \(\lambda\) and their associated probabilities for the example in Section 4.1.3.

circuit, we can say that \(1/2\) of the time, \(\lambda = \frac{1}{2}\) will contribute to \(P(\text{detected}|s_{a1} \text{ test})\), while
\(1/2\) of the time, \(\lambda = \frac{1}{2}\) will contribute to \(P(\text{detected}|s_{a0} \text{ test})\). Hence in the case of this
example we can say that \(P(\text{detected}|s_{a0} \text{ test}) = \alpha = \frac{1}{4} + \frac{1}{48} + \frac{1}{48} + \frac{1}{48} + \frac{1}{2} \times \frac{1}{6} = 0.5\). Thus,
\(P(\text{detected}|s_{a1} \text{ test}) = \beta = 0.5\) also. Now, we showed earlier that when the logic values
on the surrounding wires during one test are independent of the logic values on the wires
during another test, that is, when \(\alpha = (1 - \beta)\), as in the case of this model, then we have
the worst case of detection when \(\alpha = \beta = 0.5\). The primary assumption in this model was
that the bias voltage is the logic threshold voltage and from that the model gives us the
worst case of detection.
Chapter 5

Conclusions and future work

5.1 Conclusions

This thesis provides an initial framework for the investigation of detecting interconnect break defects. We first modeled the conditions required for a stuck-at test to detect interconnect breaks in a circuit and did a worst-case analysis of the probability of detection, considering both independence and dependence of the logic values on the wires. Using n-detection principles, we calculated the minimum number of test vectors required to detect all breaks in the circuit with a specified confidence level, given worst-case values for $\alpha$ and $\beta$.

To enhance the understanding of the faulty behavior of the circuit, we constructed a detailed probabilistic model based on the length distribution of the wires surrounding the floating wire. With certain simplifying assumptions, we used this model to compute the detection probabilities of the break using stuck-at-0 and stuck-at-1 tests. From this model we showed that we have the worst case of detection when the bias voltage is the
logic threshold voltage

5.2 Future work

In future work, we could consider the effect on $\alpha$ when trapped charge has a non-zero value and the bias voltage is different from the logic threshold voltage. Thus, we could analyze $\alpha$ as a function of the bias voltage. We can use this to get a more accurate bound on the required number of tests to detect all breaks with a specified confidence level.

In this thesis, we have considered in detail the cause and effect of the interdependence of the surrounding wires on their logic values, but we have not incorporated this dependence into the length distribution model. In future work we could address this issue.
Bibliography


